

AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [0014] with the following new paragraph [0014].

[0014] FIG. 1 is a block diagram illustrating a structure of a semiconductor device with a speed binning test circuit that performs a speed-binning test, according to an exemplary embodiment of the present invention. Referring to FIG. 1, the semiconductor device, which in FIG. 1 is embodied as a chip, for example, may include a plurality of signal input/output (I/O) pins 101-108, which are the same as those installed in a general semiconductor device, for example. Signals may be input to the signal I/O pins from a core circuit 110, and/or signals may be output from the signal I/O pins to the core circuit 110. The core circuit 110 performs given functions using its logic circuit and receives/outputs signals from/to the plurality of signal I/O pins.

Please replace paragraph [0018] with the following new paragraph [0018].

[0018] FIG. 2 is an exemplary block diagram of the first through fourth speed correlation circuits 170 through 150 shown in FIG. 1. Referring to FIG. 2, the first through fourth speed correlation circuits 120 through 150 are installed in a chain structure around the boundary of core circuit 110 and include given (known or determined in advance) unit delay circuits, i.e., inverter circuits. However, the unit delay circuits according to the exemplary embodiments of the present invention are not limited to inverter circuits. The unit delay circuits may embodied as any circuit capable of inverting input signals and outputting an inverted signal, and/or as buffers capable of outputting signals having the same phases as signals input thereto. However, if the unit delay circuits are buffers, at least one of the unit delay circuits should be an inverter circuit so that the chain structure can operate as a ring oscillator.

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Please replace paragraph [0020] with the following new paragraph [0020].

[0020] Referring to FIG. 2, the number of inverter circuits of the first group are represented as $(N+1)$; those of the second group as $2N$, those of the third group as $3N$, and those of the fourth group as $5N$. The number of inverter circuits in first group is set at $N+1$ so that the total number of inverter circuits in all four groups is an odd number. By having an odd number of total inverter circuits, the chain structure may act as a ring oscillator. The ratio of numbers of inverter circuits of the first through fourth groups may be approximately $1N:2N:3N:5N$ when N may be several tens or several hundreds of inverter circuits. The parameters a , b , c , and d of equation (1) may be any numbers, so long as the numbers are different from each other. It may be easier to evaluate the influence of on-chip variations if a , b , c , and d are set as different prime numbers.

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